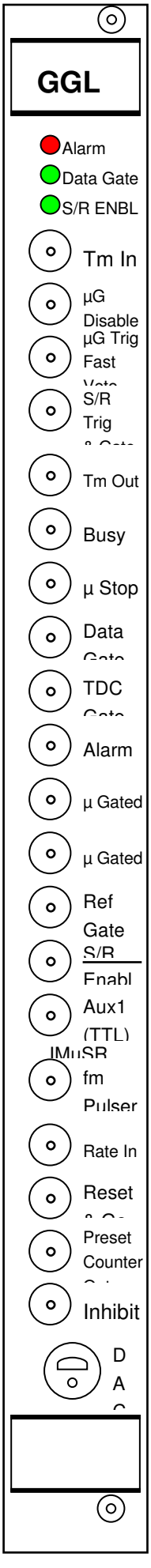
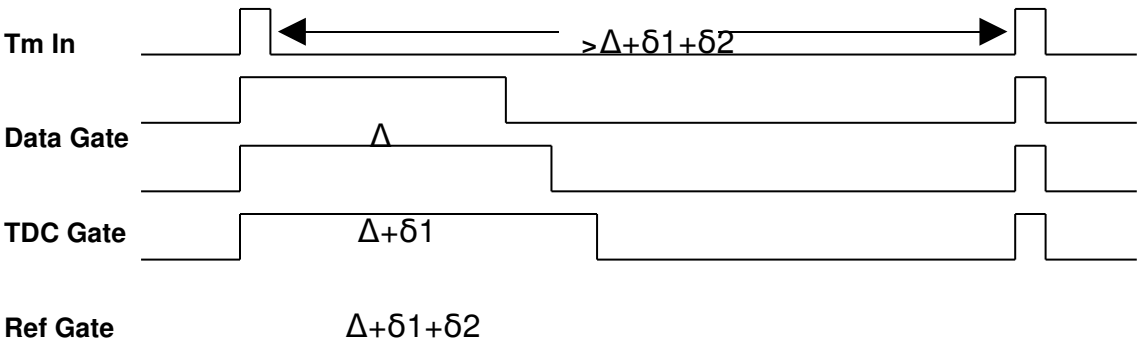


µSR VME GATE GENERATOR LOGIC Module

General Description

The VME Gate Generator Logic Module (GGL) was designed to generate the following three gate pulses.



20ns < Δ < 20.47µs 20ns < δ1, δ2 < 1.27µs

Once the **Data Gate**, the **TDC Gate** and the **Ref Gate** has been triggered by **Tm In** pulse, another **Tm In** pulse occurring before the end of **Ref Gate** will not extend any of the three gate pulses. Also, a **Tm In** pulse will trigger the three gate pulses only after Δ+δ1+δ2 seconds from the last **Tm In** pulse.

In addition, a 32-bit down counter capable at running at 10MHz was implemented. An active signal will indicate that the count value has reached zero and no pulses will be allowed thru the counter. The count value can be reset at any time via the front panel interface or via VME.

A variable period and duty cycle square wave generator was implemented. The period ranges from 0.4 milliseconds to 13.107 seconds.

A 16-bit DAC was also implemented. Six ranges are available: 0 to +5V, 0 to +10V, -2.5V to +2.5V, -5V to +5V, -10V to +10V and -2.5V to +7.5V. All output

ranges can drive up to 100 milliamperes. Range selection is performed via a VME register.

VME Interface SLAVE – A16, D16, D8 (OE)

The GGL requires a 16-bit address space. Jumpers on the printed circuit board configure the base address selection.

Address Modifier Selection

The GGL will only respond to A16 address cycles.
Short Supervisory & short nonprivileged access - 0x2D, 0x29

Base Address Selection

Each jumper corresponds to address bits A15 – A5 on the VME address bus. Installing a jumper for each address bit will select a 0 (low) for the corresponding VME address bit.

Table 1 Base Address Selection

Jumpers Installed (X)											Address Range
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	
X	X	X	X	X	X	X	X	X	X	X	0000 – 001F
-	X	X	X	X	X	X	X	X	X	X	***8000 – 801F***
-	-	X	X	X	X	X	X	X	X	X	C000 – C01F
-	-	-	X	X	X	X	X	X	X	X	E000 – E01F
-	-	-	-	X	X	X	X	X	X	X	F000 – F01F
-	-	-	-	-	X	X	X	X	X	X	F800 – F81F
-	-	-	-	-	-	X	X	X	X	X	FC00 – FC1F

Input Description

Inputs are: **Tm In, µG Disable, µG Trig Fast Veto, S/R Trig & Gate, Rate In, Reset & Go**.

All inputs accept NIM levels. **Tm In** is not 50 Ω terminated. To see a true NIM level, the user must terminate at **Tm Out** or plug **Tm Out** into a 50 Ω terminated NIM input.

Digital Output Description

Outputs are: **Tm Out, Busy, µ Stop, Data Gate, TDC Gate, Alarm, µ Gated, Ref Gate, S/R Enable, Aux1, fm Pulser, Preset Counter Out, Inhibit**.

All digital outputs with the exception of **AUX1** drive NIM levels. **AUX1** is a TTL output with a 50 Ω drive.

µG Trig Fast Veto Setup

The minimum setup time is 3ns with respect to the **Tm In** signal. The pulse width of the **µG Trig Fast Veto** should be set to 5ns (assuming 3ns setup time). Veto efficiency goes to zero with a 2ns setup time.

Table 2 Default Register Values

Function	Address	Value

Main Delay (MSB)	00	03
Main Delay (LSB)	01	E8
Delta 1 Delay	02	1E
Delta 2 Delay	03	32
VME S/R Enable	04	00
DAC Range Control	05	00
DAC Setpoint (MSB)	06	00
DAC Setpoint (LSB)	07	00
Counter Preset Value (MSB, Byte 3)	08	00
Counter Preset Value (Byte 2)	09	98
Counter Preset Value (Byte 1)	0A	96
Counter Preset Value (LSB, Byte 0)	0B	80
Counter Readback Value (MSB, Byte 3)	0C	00
Counter Readback Value (Byte 2)	0D	98
Counter Readback Value (Byte 1)	0E	96
Counter Readback Value (LSB, Byte 0)	0F	80
Pulser HI Time Set Value (MSB)	10	00
Pulser HI Time Set Value (LSB)	11	02
Pulser LO Time Set Value (MSB)	12	00
Pulser LO Time Set Value (LSB)	13	02
Pulser enable	14	00
VME GGL Alarm	15	00
Not Used	16	00
Not Used	17	00
Not Used	18	00
Not Used	19	00
Not Used	1A	00
Not Used	1B	00
Not Used	1C	00
Counter Reset	1D	00
Not Used	1E	00
VME Register Reset	1F	00

11-Bit Δ Delay Register: 00, 01 (Default: 03E8H)

These registers will respond to a byte or a word access.

ADR	$xxxxxx00 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R/W	R/W	R/W
RESET	0	0	0	0	0	0	1	1

ADR	$xxxxxx01 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	1	1	0	1	0	0	0

Δ delay = register value x 10ns

By default, Δ delay is 10µs. Value in register **MUST** be greater than or equal to 2.

7-Bit δ1 Delay Register: 02 (Default: 1EH)

This register will respond to a byte or a word access.

ADR	$xxxxxx02 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	1	1	1	1	0

δ1 delay = register value x 10ns

By default, δ1 delay is 300ns. Value in register **MUST** be greater than or equal to 2.

7-Bit δ2 Delay Register: 03 (Default: 32H)

This register will respond to a byte or a word access.

ADR	$xxxxxx03 (Bits 7-0)

BIT	7	6	5	4	3	2	1	0
OPER	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	1	1	0	0	1	0

Δ2 delay = register value x 10ns

By default, δ2 delay is 500ns. Value in register **MUST** be greater than or equal to 2.

VME S/R Enable Register: 04 (Default: 00H)

This register will respond to a byte or a word access.

ADR	$xxxxxx04 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

AUX1 = bit1 **xor** (**not** (Ref Gate **and** bit0))

S/R Enable = bit0 **xor** bit2

DAC Range Control Register: 05 (Default: 00H)

This register will respond to a byte or a word access.

ADR	$xxxxxx05 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

The DAC output range is +5V with an output voltage of 0V when powered initially.

Bit3..Bit 0:
000B: 0 to +5V.
001B: 0 to +10V.
010B: -5V to +5V.
011B: -10V to +10V
100B: -2.5V to +2.5V
101B: -2.5V to +7.5V

DAC Setpoint Register: 06, 07 (Default: 0000H)

These registers will respond to a byte or a word access.

ADR	$xxxxxx06 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADR	$xxxxxx07 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

	0 to +5V	**0 to +10V**	**-5V to +5V**	**-10V to +10V**	**-2.5V to +2.5V**	**-2.5V to +7.5V**
FFFFH	+5.00V	+10.0V	+5.00V	+10.0V	+2.50V	+7.50V
C000H	+3.75V	+7.50V	+2.50V	+5.00V	+1.25V	+5.00V

8000H	+2.50V	+5.00V	0V	0V	0V	+2.50V
4000H	+1.25V	+2.50V	-2.50V	-5.00V	-1.25V	0V
0000H	0V	0V	-5.00V	-10.0V	-2.50V	-2.50V

32-Bit Down Counter Preset Register: 08,09,0A,0B (Default: 00989680H)

These registers will respond to a byte or a word access.

ADR	$xxxxxx08 (Bits 31-24)							
BIT	31	30	29	28	27	26	25	24
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADR	$xxxxxx09 (Bits 23-16)							
BIT	23	22	21	20	19	18	17	16
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	0	1	1	0	0	0

ADR	$xxxxxx0A (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	0	1	0	1	1	0

ADR	$xxxxxx0B (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	0	0	0	0	0	0

The default value is 10 million counts. The counter will stop when the count value has reached zero. The user can reset of the counter thru VME or thru the front panel interface.

32-Bit Down Counter Readback Register: 0C,0D,0E,0F (Default: 00989680H)

These registers will respond to a byte or a word access.

ADR	$xxxxxx0C (Bits 31-24)							
BIT	31	30	29	28	27	26	25	24
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

ADR	$xxxxxx0D (Bits 23-16)							
BIT	23	22	21	20	19	18	17	16
OPER	R	R	R	R	R	R	R	R
RESET	1	0	0	1	1	0	0	0

ADR	$xxxxxx0E (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R	R	R	R	R	R	R	R
RESET	1	0	0	1	0	1	1	0

ADR	$xxxxxx0F (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R
RESET	1	0	0	0	0	0	0	0

These register displays the current count value of the 32-bit down counter.

Pulser HI Time Setpoint Register: 10, 11 (Default: 0002H)

These registers will respond to a byte or a word access.

ADR	$xxxxxx10 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADR	$xxxxxx11 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	1	0

By default, HI time is 200µs. Value in registers **MUST** be greater than or equal to 2.

Pulser LO Time Setpoint Register: 12, 13 (Default: 0002H)

These registers will respond to a byte or a word access.

ADR	$xxxxxx12 (Bits 15-8)							
BIT	15	14	13	12	11	10	9	8
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

ADR	$xxxxxx13 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	1	0

By default, LO time is 200µs. Value in registers **MUST** be greater than or equal to 2.

Pulser Enable Register: 14 (Default: 00H)

This register will respond to a byte or a word access.

ADR	$xxxxxx14 (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R/W
RESET	0	0	0	0	0	0	0	0

The Pulser is disabled when powered initially.

Bit 0: 0: Disabled.
1: Enabled.

Period = (HI Time Setpoint + LO Time Setpoint) x 0.0001 seconds.

Alarm Register: 15 (Default: 00H)

This register will respond to a byte or a word access.

ADR	$xxxxxx1D (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R	R	R	R	R	R	R	R/W
RESET	0	0	0	0	0	0	0	0

Bit 0: 0: Disabled.
1: Enabled.

32-Bit Down Counter Reset Register: 1D (Default: 00H)

This register will respond to a byte or a word access.

ADR	$xxxxxx1D (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Write cycle will reload 32-bit down counter with the value in the counter set registers. Value read from this register is always zero.

VME Reset Control Register: 1F (Default: 00H)

This register will respond to a byte or a word access.

ADR	$xxxxxx1F (Bits 7-0)							
BIT	7	6	5	4	3	2	1	0
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0

Write cycle will reset all VME registers to default values. However, the DAC output voltage and range will remain unchanged and not reflected in the register values.

Block Diagram of Module Operation